

Testing Linearity of the LTC2400 24-Bit No Latency $\Delta\Sigma$ ™ A/D Converter

Help from the Nineteenth Century

by Jim Williams

Introduction

Verifying the linearity of the LTC2400 analog to digital converter requires special considerations. Typical nonlinearity is only 2ppm (0.0002%). Bench testing this necessitates some form of voltage source that produces equal amplitude output steps for incremental digital inputs. Additionally, for measurement confidence, it is desirable that the source be substantially more linear than the 2ppm requirement. This is, of course, a stringent demand and painfully close to the state of the art.

The most linear "D to A" converter is also one of the oldest: Lord Kelvin's Kelvin-Varley divider (KVD), in its most developed form, is linear to 0.1ppm. This manually switched device features ten million individual dial settings arranged in seven decades. It may be thought of as a 3-terminal potentiometer with fixed "end-to-end" resistance and a 7-decade switched wiper position (Figure 1).

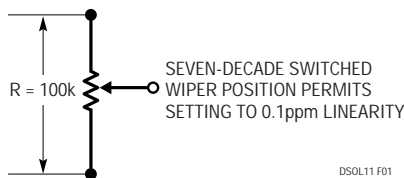


Figure 1. Conceptual Kelvin-Varley Divider

The actual construction of a 0.1ppm KVD is more artistry and witchcraft than science. The market is relatively small, the number of vendors few and resultant price high. Imagine paying \$13,000 for a bunch of switches and resistors. If this seems offensive, try building and certifying your own KVD. Figure 2 shows a detailed schematic.

The KVD shown has a 100k Ω input impedance. A consequence of this is that wiper output resistance is high and varies with setting. As such, a very high input resistance

follower is required to unload the KVD without introducing significant loading error. Now, our KVD looks like Figure 3.

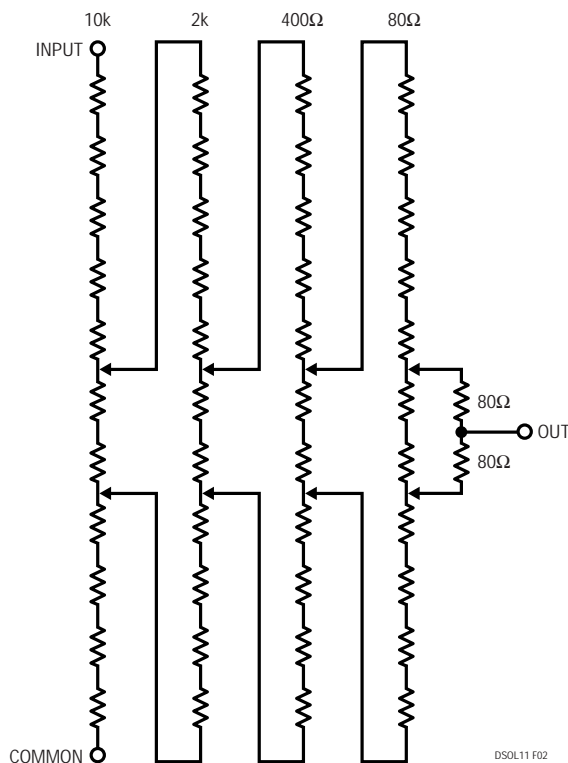


Figure 2. A 4-Decade Kelvin-Varley Divider. Additional Decades Are Implemented By Opening Last Switch, Deleting Two Associated 80 Ω Values and Continuing $\div 5$ Resistor Chains

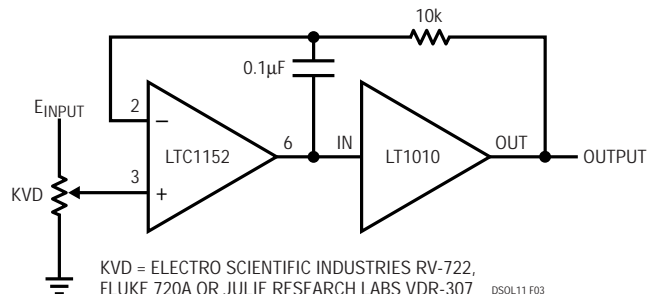


Figure 3. KVD with Buffer Gives Output Drive Capability

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
No Latency $\Delta\Sigma$ is a trademark of Linear Technology Corporation.

Design Solutions 11

This schematic is deceptively simple. In practice, construction details are crucial. Parasitic thermocouples (Seebeck effect), layout, grounding, shielding, guarding, cable choice and other issues affect achievable performance. In fact, as good as the chopper-stabilized LTC1152 is with respect to drift, offset, bias current and CMRR, selection is required if we seek sub-ppm nonlinearity performance. Figure 4, an error budget analysis, details some of the selection criteria.

In Figure 5, we can add offset trim, a second KVD and a stable voltage source to drive the main KVD. Additionally, an ensemble of three HP3458A voltmeters monitor the output.

The offset trim bleeds a small current into the main KVD ground return, producing a few microvolts of offset-trim range. This functionally trims out all sources of zero error (amplifier offsets, parasitic thermocouple mismatches and the like), permitting a true zero volt output when the main KVD is set to all zeros.

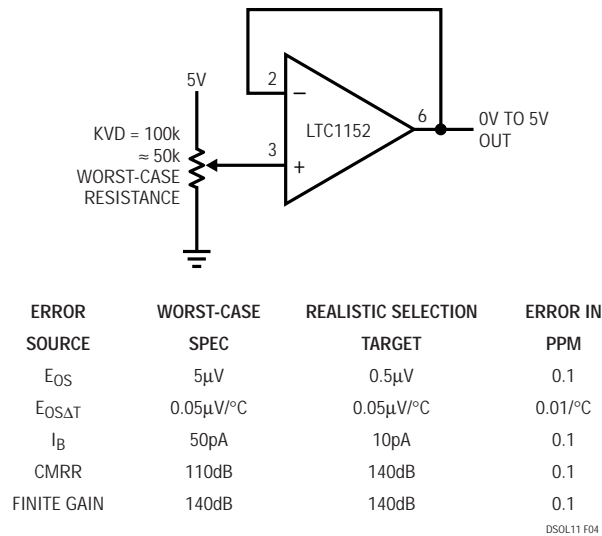


Figure 4. Error Budget Analysis for the KVD Buffer. Selection Permits \approx 0.4ppm Predicted Linearity Error

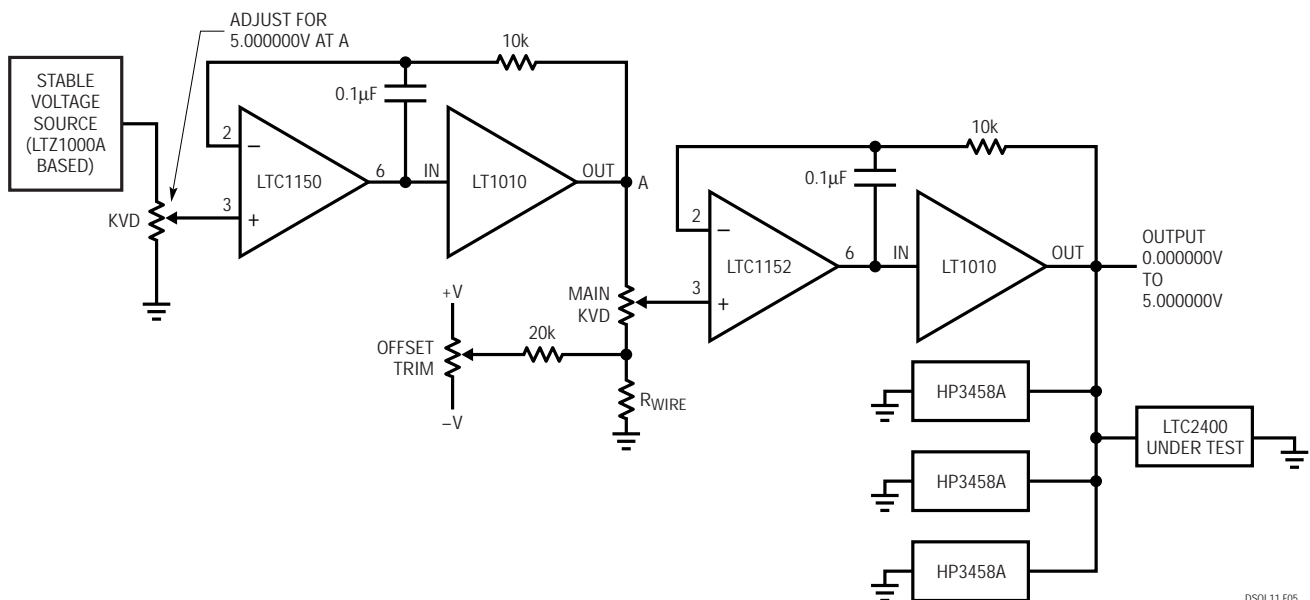


Figure 5. Simplified High Linearity Voltage Source

The voltmeters, specified for <1ppm nonlinearity on the 10V range, “vote” on the source’s output. Figure 6 is a more detailed schematic and Figure 7 highlights issues and concerns.

When studying the approach used, it is essential to differentiate between linearity and absolute accuracy. This eliminates concerns with absolute standards, permitting certain freedoms in the measurement scheme. In particular, although single-point grounding was used, remote sensing was not. This is a deliberate choice, made to minimize the number of potential error-causing parasitic thermocouples in the signal path.

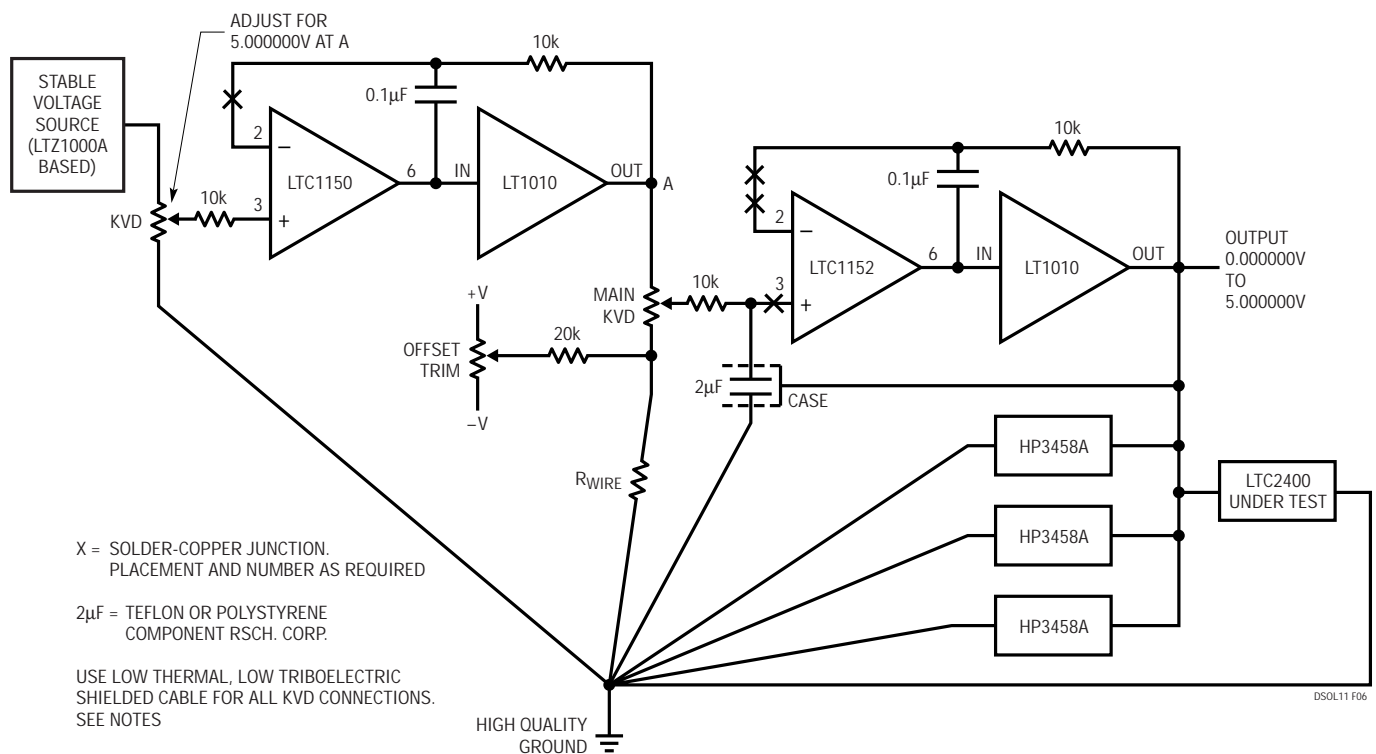


Figure 6. Complete High Linearity Voltage Source

- OFFSET TRIM VIA DRIVING KVD RETURN WIRE
- HIGH QUALITY GROUND
- CABLE CHOICE — GUILDLINE #SCW, KEITHLEY SC-93
- LOW THERMAL LUGS, BANANAS – HP11053, 8.11074
- CRUSH LUGS FOR KVD AND DVM CONNECTIONS
- DELIBERATE SOLDER-COPPER JUNCTIONS
- DRIVEN CASE GUARDS AGAINST CAPACITOR SURFACE LEAKAGE
- “MICROVOLT MAINTENANCE” (DE-OXIT, CAIG LABS)

DSOL11 F07

Figure 7. Voltage Source Notes and Special Attention Areas

Design Solutions 11

Results

This KVD-based, high linearity voltage source has been in use in our lab for about a year. During this period, the total linearity uncertainty defined by the source and its monitoring voltmeters has been just 0.3ppm (see Figure 8). This is almost ten times better than the LTC2400's 2ppm specification, promoting confidence in our measurements.

Acknowledgments

The author is indebted to Lord Kelvin and to Warren Little of the C. S. Draper Laboratory (formerly the M. I. T. Instrumentation Laboratory) standards lab. Warren taught me, with great patience, the wonders of KVDs some thirty years ago and I am still trading on his efforts.

- VERIFY KVD LINEARITY BY INTERCOMPARISON AND INDEPENDENT CAL. LAB.
- TAKE WORST-CASE VOLTMETER ENSEMBLE DEVIATIONS OVER 0V TO 5V, EVERY 0.5V
- 100 RUNS (10 PER DAY, ONCE PER HOUR)
- INDICATED RESULT IS 0.3ppm NONLINEARITY

DSOL11 F08

Figure 8. Linearity Testing Using Repeated Trials with "Voting" Voltmeters